計算機組織資格考題（Spring 2019）

1. (20%) For the following we consider instruction encoding for instruction set architectures.
   a. Consider the case of a processor with an instruction length of 12 bits and with 32 general-purpose registers so the size of the address fields is 5 bits. Is it possible to have instruction encodings for the following? Explain your answer.
      - 3 two-address instructions
      - 30 one-address instructions
      - 45 zero-address instructions
   b. Assuming the same instruction length and address field sizes as above, determine if it is possible to have instruction encodings for the following? Explain your answer.
      - 3 two-address instructions
      - 31 one-address instructions
      - 35 zero-address instructions

2. (20%) Explain energy-delay product (EDP and power-delay product (PDP) and explain why EDP is a better metric than PDP to compare different designs.

3. (30%) For the following cache optimization, explain (1) what can be improved? miss rate, miss penalty, or hit time? (2) explain why
   a. Larger Block Size: Reduce Miss Rate
   b. Larger Caches: Reduce Miss Rate
   c. Higher Associativity: Reduce Miss Rate
   d. Multilevel Caches: Reduce Miss Penalty
   e. Faster L1 cache, L2 has less miss penalty than memory
   f. Giving Priority to Read Misses over Writes: Miss Penalty
   g. Write to buffer first, and no need wait for write for dirty block replacement
   h. Avoiding Address Translation during indexing of the cache: hit time
   i. TLB translation is parallel to cache access time

4. (30%) Assume that individual stages of the datapath have the following latencies:

IF	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

   Also, assume that instructions executed by the processor are broken down as follows:

Alu	beq	lw	Sw
45%	20%	20%	15%

   a. What is the clock cycle time in a pipelined and non-pipelined processor?
   b. What is the total latency of an LW instruction in a pipelined and non-pipelined processor?
   c. If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor?